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EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
02/10/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/756,939	PARK, JIN-HO	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In a response dated, January 19th, 2010, the Applicant amended claims 1 and 7. Currently claims 1-11, 14-17 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 19th, 2010 has been entered.

Response to Arguments

3. Applicant's arguments filed January 19th, 2010 have been fully considered but they are not persuasive.

4. On pages 10-11 of the Remarks the Applicants argue that the Kawaguchi reference does not teach wherein the output instruction signal line is connected to the timing controller through the data TCP. As support for this argument the Applicant points to the figure 30 embodiment of Kawaguchi.

5. The Examiner agrees that the figure 30 embodiment does not teach such a limitation. Other embodiments do, however, appear to disclose such a limitation. For example, figure 20 discloses a timing controller (191) on a printed circuit board (111B). Furthermore, it seems clear that the output instruction signal lines are supplied to the data drivers via the data TCP (104A). This embodiment is more specifically mapped to

the claim limitations below which describe the manner of combination and provide motivation for the proposed combination.

6. As discussed above, and shown below, the previously cited Kawaguchi is seen as disclosing the newly added limitations. As such the rejections are updated to reflect this.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katagawa (US 7,079,105) in view of Nakamura et al. (US 7,136,058) and further in view of Kawaguchi et al. (US 5,592,199).

With respect to claim 1, Katagawa discloses, an LCD apparatus comprising:

an LCD panel (fig. 10) displaying images (col. 12, lines 44-46) and including:

a first substrate (14 in fig. 1);

a second substrate facing the first substrate (1 in figs. 1 and 10), a plurality of pixels being provided on the second substrate (fig. 1; col. 4, lines 45-64);

a common electrode disposed on the first substrate (col. 5, lines 8-12);

gate lines (2 in figs. 1 and 10) disposed on the second substrate and opposing the common electrode (col. 4, lines 53-55; fig. 1), the gate lines receiving a gate driving signal (Gn in fig. 11, for example);

data lines for supplying image data signals to the pixels (4 in figs. 1 and 10); and

an output instruction signal line (70 in fig. 10) disposed on the second substrate (fig. 10) transmitting an output instruction signal;

a data driver (16-1-n in fig. 10) disposed on a data tape carrier package (TCP) (col. 5, lines 20-28);

a gate driver (18-1-n in fig. 10) outputting a gate driving signal to the LCD panel; and

a timing controller (20 in fig. 10) providing a first control signal (26 in fig. 10) to the gate driver so as to control an output of the gate driving signal and providing the output instruction signal (col. 11, lines 49-51) to the data driver via the output instruction signal line (70 in fig. 10) to delay the output instruction signal depending on a capacitive load (col. 11, lines 1-4) and depending on a resistive load formed by the output instruction signal line (col. 11, lines 59-65),

wherein the output instruction signal line is disposed between the data TCP and the gate lines (fig. 10; col. 11, lines 44-47), and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal (col. 11, lines 59-65; col. 12, lines 17-42).

Katagawa is silent as to the source of the capacitive load delay on the instruction signal line.

Katagawa does not expressly disclose that the output instruction signal line is disposed opposite the common electrode.

Nakamura discloses, an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);

gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Katagawa are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal line of Katagawa so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

To further explain, the proposed combination, it is seen as clear that upon locating the output instruction signal line of Katagawa under the common electrode as

taught by Nakamura, this would result in the capacitance between the common electrode and the output instruction signal line being the sole capacitive load delay component.

Neither Katagawa nor Nakamura expressly disclose locating the timing controller on a printed circuit board or that the output instruction signal line is connected to the timing controller through the data TCP.

Kawaguchi discloses, a timing controller (191 in fig. 20) on a printed circuit board (111B in fig. 20),

wherein an output instruction signal line (173 in fig. 20, for example) is connected to the timing controller through a data TCP (104A in fig. 20).

Kawaguchi, Nakamura and Katagawa are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the so arranged TCPs and printed circuit boards of Kawaguchi for the output instruction signal line of Nakamura and Katagawa.

The motivation for doing so would have been to reduce costs and decrease weight and manufacturing time (Kawaguchi; col. 25, line 61 - col. 26, line 14).

With respect to claim 2, Nakamura, Kawaguchi and Katagawa disclose, the LCD apparatus of claim 1 (see above).

Katagawa further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 10).

With respect to claim 3, Nakamura, Kawaguchi and Katagawa disclose, the LCD apparatus of claim 2 (see above).

Neither Katagawa nor Nakamura expressly disclose a plurality of signal transmission members.

Kawaguchi discloses, a plurality of signal transmission members (246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel,

wherein an output instruction signal line (231 in fig. 32, for example) receives the output instruction signal from the timing controller via one of the signal transmission members (note the connection of 231 with 242 and 240 in fig. 32).

Kawaguchi, Nakamura and Katagawa are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the so arranged signal transmission members of Kawaguchi for the output instruction signal line of Nakamura and Katagawa.

The motivation for doing so would have been increase the ruggedness of the display and improve reliability (Kawaguchi; col. 4, lines 6-24).

With respect to claim 4, Nakamura, Kawaguchi and Katagawa disclose, the LCD apparatus of claim 3 (see above).

Katagawa further discloses, wherein the LCD panel comprises:

the gate lines (2 in fig. 1) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a

second direction substantially perpendicular to the first direction (fig. 1, for example); and

a plurality of data lines (4 in fig. 1) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction (fig. 1).

With respect to claim 5, Nakamura, Kawaguchi and Katagawa disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines (fig. 10).

With respect to claim 6, Nakamura, Kawaguchi and Katagawa disclose, the LCD apparatus of claim 4 (see above).

Katagawa further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (fig. 1), and the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (figs. 7-9, 11-12; col. 12, lines 30-36).

With respect to claim 7, Katagawa discloses, an LCD apparatus comprising:

an LCD panel (fig. 10) displaying images (col. 12, lines 44-46) and including:

a first substrate (14 in fig. 1);

a second substrate facing the first substrate (1 in figs. 1 and 10), a plurality of pixels being provided on the second substrate (fig. 1; col. 4, lines 45-64);

a common electrode disposed on the first substrate (col. 5, lines 8-12);

gate lines (2 in figs. 1 and 10) disposed on the second substrate and opposing the common electrode (col. 4, lines 53-55; fig. 1), the gate lines receiving a gate driving signal (Gn in fig. 11, for example);

data lines for supplying image data signals to the pixels (4 in figs. 1 and 10); and

an output instruction signal line (70 in fig. 10) disposed on the second substrate (fig. 10) transmitting an output instruction signal;

a data driver (16-1-n in fig. 10) disposed on a data tape carrier package (TCP) (col. 5, lines 20-28);

a gate driver (18-1-n in fig. 10) outputting a gate driving signal to the LCD panel; and

a timing controller (20 in fig. 10) providing a first control signal (26 in fig. 10) to the gate driver so as to control an output of the gate driving signal and providing the output instruction signal (col. 11, lines 49-51) to the data driver via the output instruction signal line (70 in fig. 10) to delay the output instruction signal depending on a capacitive load (col. 11, lines 1-4) and depending on a resistive load formed by the output instruction signal line (col. 11, lines 59-65),

wherein the output instruction signal line is disposed between the data TCP and the gate lines (fig. 10; col. 11, lines 44-47), and

wherein the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed such that a delayed time of the image signal is substantially equal to a delayed time of the gate driving signal (col. 11, lines 59-65; col. 12, lines 17-42).

Katagawa is silent as to the source of the capacitive load delay on the instruction signal line.

Katagawa does not expressly disclose that the output instruction signal line is disposed opposite the common electrode.

Nakamura discloses, an LCD apparatus comprising:

a first substrate, and a second substrate facing the first substrate (col. 4, lines 10-19);

a common electrode disposed on the first substrate (col. 4, lines 17-19);

gate lines disposed on the second substrate and opposing the common electrode (col. 4, lines 10-19); and

signal lines (P1 in fig. 14; and C4, C5 wiring in fig. 15) disposed on the second substrate and opposing the common electrode such that the signal lines have a capacitive load (fig. 14-15; the signal lines will inherently have a capacitive load due to being overlapped with the common electrode in a manner identical to the Applicant's invention).

Nakamura and Katagawa are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to arrange the output instruction signal line of Katagawa so as to overlap the common electrode as taught by Nakamura.

The motivation for doing so would have been to reduce the frame size of the LCD, resulting in a more portable display (Nakamura; col. 15, lines 42-50).

To further explain, the proposed combination, it is seen as clear that upon locating the output instruction signal line of Katagawa under the common electrode as taught by Nakamura, this would result in the capacitance between the common electrode and the output instruction signal line being the sole capacitive load delay component.

Neither Katagawa nor Nakamura expressly disclose a plurality of signal transmission members, locating the timing controller on a printed circuit board or that the output instruction signal line is connected to the timing controller through the data TCP.

Kawaguchi discloses, a timing controller (191 in fig. 20) on a printed circuit board (111B in fig. 20), and

a plurality of signal transmission members (246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel,

wherein an output instruction signal line (231 in fig. 32, for example) provides the output instruction signal to the data driver via one of the signal transmission members (note the connection of 231 with 242 and 240 in fig. 32),

wherein an output instruction signal line (173 in fig. 20, for example) is connected to the timing controller through a data TCP (104A in fig. 20).

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the so arranged signal transmission members of Kawaguchi for the output instruction signal line of Nakamura and Katagawa.

The motivation for doing so would have been increase the ruggedness of the display and improve reliability (Kawaguchi; col. 4, lines 6-24).

With respect to claim 8, Katagawa, Nakamura and Kawaguchi disclose, the LCD apparatus of claim 7 (see above).

Katagawa further discloses, wherein the LCD panel comprises:

the gate lines (2 in fig. 1) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction (fig. 1, for example); and

a plurality of data lines (4 in fig. 1) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction (fig. 1).

With respect to claim 9, Katagawa, Nakamura and Kawaguchi disclose, the LCD apparatus of claim 8 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines (fig. 10).

With respect to claim 10, Katagawa, Nakamura and Kawaguchi disclose, the LCD apparatus of claim 9 (see above).

Katagawa further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (fig. 1), and the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (figs. 7-9, 11-12; col. 12, lines 30-36).

With respect to claim 11, Katagawa, Nakamura and Kawaguchi disclose, the LCD apparatus of claim 7 (see above).

Katagawa further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 10).

With respect to claim 14, McCartney, Nakamura and Kawaguchi disclose, the LCD apparatus of claim 1 (see above).

Kawaguchi discloses, a plurality of signal transmission members (246, 248 in fig. 32; for example) electrically connecting the data driver with the LCD panel,

wherein an output instruction signal line (231 in fig. 32, for example) receives the output instruction signal from the timing controller via one of the signal transmission members (note the connection of 231 with 242 and 240 in fig. 32).

Kawaguchi, Nakamura and Katagawa are analogous art because they are both from the same field of endeavor, namely LCD driver circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the so arranged signal transmission members of Kawaguchi for the output instruction signal line of Nakamura and Katagawa.

The motivation for doing so would have been increase the ruggedness of the display and improve reliability (Kawaguchi; col. 4, lines 6-24).

With respect to claim 15, Nakamura, Kawaguchi and Katagawa disclose the LCD apparatus of claim 1 (see above).

Katagawa, when combined with Nakamura, further discloses wherein capacitive and resistive loads of the gate lines and the output instruction signal line are substantially equal to each other (Katagawa; col. 12, lines 25-36, col. 11, lines 59-65).

With respect to claim 16, Nakamura, Kawaguchi and Katagawa disclose the LCD apparatus of claim 1 (see above).

Katagawa, when combined with Nakamura, further discloses wherein a delay of providing the output instruction signal to the data driver is substantially equal to the delay of the gate driving signal (Katagawa; col. 12, lines 25-36, col. 11, lines 59-65).

With respect to claim 17, Nakamura, Kawaguchi and Katagawa disclose the LCD apparatus of claim 1 (see above).

Katagawa further discloses, wherein a portion of the output signal line is disposed on the data driver (fig. 10; seems clear that a portion of 70 is included in the data driver).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/
Primary Examiner, Art Unit 2629
2/8/2011